REMARKS

This application was filed with 21 claims. Claims 1-21 have been rejected. Claims 5-6, 12, and 14 have been amended. No claims have been canceled. New Claims 22-23 have been added. Therefore, Claims 1-23 are pending in the Application. Reconsideration of the application based on the amended claims and the arguments submitted below is respectfully requested.

Claim Rejections - 35 U.S.C. §102(b)

Claims 15-20 have been rejected under 35 U.S.C. §102(b) as being unpatentable based on U.S. Patent No. 4,330,809 issued to Stanley. Applicant respectfully traverses this rejection because these claims include a claim limitation that is not taught by Stanley. As a result, Stanley cannot anticipate these claims and this rejection should be withdrawn.

Claim 15 is directed to a protection method that includes the step of generating ***a power estimate*** of power dissipated by a power transistor. Stanley does not teach a protection method that includes this step. Stanley teaches a protection method that includes the step of generating a signal that is representative of ***the actual power*** dissipated by a power transistor, not an estimate of that power as required by this claim. Stanley, col. 2, ll. 12-15; Application as originally filed, p. 23, ll. 1-7. Thus, Stanley does not teach this limitation and cannot anticipate this claim.

Claims 16-20 are dependent claims that depend on Claim 15 and include all of the limitations required by that claim, including the limitation relating to the

step of generating a power estimate of power dissipated by a power transistor. As indicated above, Stanley does not teach this limitation. Accordingly, Claims 16-20 are not anticipated by Stanley for the same reason that Claim 15 is not anticipated by Stanley.

Claim 16 is also patentable over Stanley because it is directed to a protection method that includes the step of adjusting the filtered power estimate so that it varies as a function of power transistor operating temperature. Stanley does not teach this step. Col. 2, ll. 27-33 of Stanley, cited by the patent examiner in support of this rejection, does not indicate otherwise. This portion of Stanley simply indicates that the instantaneous sensed die temperature is fed to a temperature comparator that is programmed to react to a selected maximum die temperature and to produce a responsive signal that causes the controlling input to the power transistor to be reduced. This portion of Stanley does not discuss adjusting the filtered power estimate so that it varies as a function of power transistor operating temperature as required by this claim.

Claim 18 is also patentable over Stanley because it is directed to a protection method that includes a power transistor control signal that causes the power transistor to reduce its power dissipation by reducing power supply voltage applied to the power transistor. The examiner cites col. 3, ll. 14-16 of Stanley in support of this rejection. This portion of Stanley, however, indicates that the signal representative of the temperature of the power transistor heat sink is combined with the signal representative of the temperature differential between the

transistor die and the heat sink to generate a signal that is representative of the temperature of the transistor die. This portion does not indicate that the power supply voltage applied to the transistor is reduced in order to reduce the power dissipated by the power transistor as required by this claim.

Claim 20 is also patentable over Stanley for similar reasons. Claim 20 is directed to a protection method that includes a power transistor control signal that causes the power transistor to reduce its power dissipation by reducing power supply voltage applied to the power transistor and reducing base current flowing into the power transistor. The portion of Stanley cited by the examiner in support of this rejection, col. 3, ll. 14-31, does not indicate that the power dissipated by the power transistor is reduced by reducing the power supply voltage. This portion of Stanley indicates that the power dissipated by the power transistor is reduced by shunting the controlling input from the base of the power transistor.

Claim Rejections - 35 U.S.C. §103

Claims 1-11 and 13 have been rejected under 35 U.S.C. §103 as being unpatentable based on the acknowledged prior art and Stanley. Applicant respectfully traverses this rejection because all of these claims include a claim limitation that is not taught or suggested by the acknowledged prior art or Stanley. Accordingly, the rejection of these claims should be withdrawn. The rejection of Claims 5 and 6 should also be withdrawn because these claims have been amended to include additional claim limitations that are not taught or suggested by the acknowledged prior art or Stanley.

Claim 1 is directed to a protection circuit that includes a transistor maximum current limiting circuit. The acknowledged prior art and Stanley do not teach this type of circuit. The examiner indicates that Qout shown in Fig. 5 of the currently pending application is the maximum current limiting circuit required by this claim. Applicant respectfully submits that the examiner is mistaken in this regard. As explained on page 6, l. 14 of the currently pending application, ***Qout is a power transistor, not a maximum current limiting circuit***. Thus, the acknowledged prior art does not teach this limitation as indicated by the examiner.

The examiner does not indicate that Stanley teaches the maximum current limiting circuit required by this claim. Thus, Stanley does not teach this limitation either.

Claims 2-11 and 13 are dependent claims that depend on Claim 1 and include all of the limitations required by that claim, including the limitation relating to the transistor maximum current limiting circuit. As indicated above, the acknowledged prior art and Stanley do not teach this limitation. Claims 2-11 and 13, therefore, are not obvious in view of the acknowledged prior art and Stanley for the same reason that Claim 1 is not obvious in view of these references.

Claim 5 has been amended to indicate that it includes a four-slope power estimation circuit that is ***connected to a reference voltage that falls between ground and a main power transistor rail voltage***. The acknowledged prior art and Stanley do not teach or suggest the use of this type of power estimation circuit.

Thus, this claim is patentable over the acknowledged prior art and Stanley for this reason as well.

Claim 6 has been amended to indicate that it includes a multi-slope power estimation circuit that ***includes a resistor diode network connected to a reference voltage that falls between ground and a main power transistor rail voltage***. The acknowledged prior art and Stanley do not teach or suggest the use of this type of power estimation circuit. Claim 6, therefore, is patentable over the acknowledged prior art and Stanley for this additional reason.

Claim 12

Claim 12 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the acknowledged prior art in view of Stanley and Bodge. Applicant traverses this rejection, but nevertheless has amended this claim to include an additional claim limitation that is clearly not taught or suggested by acknowledged prior art, Stanley, or Bodge. Claim 12 has been amended to indicate that it includes ***a thermistor that is thermally coupled to a case of a power transistor***. The acknowledged prior art, Stanley, and Bodge do not teach or suggest the use of a thermistor thermally coupled to a case of a power transistor. Thus, the rejection of Claim 12 should be withdrawn.

Claim 14

Claim 14 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the acknowledged prior art in view of Stanley and Knudsen. Applicant traverses this rejection, but nevertheless has amended this claim to include an

additional claim limitation that is clearly not taught or suggested by the acknowledged prior art, Stanley, or Knudsen. Claim 14 has been amended to indicate that it includes ***an optocoupler that is coupled to a power supply regulation circuit in a manner that causes a power supply voltage applied to a power transistor to be reduced when the optocoupler is triggered***. The acknowledged prior art, Stanley, and Knudsen do not teach or suggest the use of an optocoupler that is coupled in this manner. Claim 14 is therefore patentable over the art relied upon by the examiner and this rejection should be withdrawn.

Claim 21

Claim 21 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Bishop in view of Wyland. Applicant respectfully traverses this rejection because these references do not teach or suggest several claim limitations required by this claim and requests that this rejection be withdrawn.

Claim 21 is directed to a method of estimating junction temperature of a transistor that includes the steps of generating a piecewise linear approximation of the transistor's power dissipation, varying the piecewise linear approximation as a function of transistor temperature, and averaging the temperature varying, piecewise linear approximation to generate an estimate of transistor junction temperature. Neither Bishop nor Wyland teach or suggest any of these steps.

Bishop is directed to a system and method for linearizing analog measurements during an analog-to-digital conversion. While it is true that Bishop discusses the use of a piecewise linear approximation technique at col. 1, ll. 33-36,

Bishop does not discuss generating ***a piecewise linear approximation of a transistor's power dissipation*** as required by this claim. Wyland, which is directed to a device for simulating thermal power dissipation in a board supporting an electronic component, likewise does not discuss a transistor's power dissipation or generating a piecewise linear approximation of this type of power dissipation. Thus, Bishop and Wyland, even if combined together as suggested by the examiner, simply do not teach or suggest the step of generating a piecewise linear approximation of a transistor's power dissipation.

The examiner cites col. 1, ll. 33-36 of Bishop and indicates that this portion of Bishop teaches the step of generating a piecewise linear approximation. The examiner then cites the lines 1-4 and 17-20 of the abstract of Wyland for its teaching that it is known to estimate the junction temperature of a transistor and indicates that it would have been obvious to one of ordinary skill in the art to use the piecewise linear approximation of Bishop to generate an estimate of power dissipated in a transistor as taught by Wyland. The problem with this argument is that Wyland, including the portions cited by the examiner, does not discuss power dissipation in a transistor or measuring that dissipation. Thus, combining the teachings of Bishop and Wyland does not result in the claimed step of generating a piecewise linear approximation of a transistor's power dissipation because neither Bishop nor Wyland mention measuring the power dissipation in a transistor.

Bishop and Wyland also do not teach or suggest the other two steps required by this claim. The examiner acknowledges that Wyland does not teach or suggest

either of these steps and relies exclusively on Bishop in this regard. Accordingly, Wyland is not discussed in any further detail and only the examiner's arguments relating to Bishop are discussed below.

The second step required by this claim is the step of varying the piecewise linear approximation as a function of transistor temperature. The examiner indicates that col. 1, ll. 14-20 of Bishop teaches this step. A review of this portion of Bishop, however, indicates that this is not the case. The cited portion reads:

> For example, these techniques may be employed to measure the voltage, in digital form, of a thermocouple, which has a non-linear temperature-voltage function. In order to obtain a true measure of temperature, however, the digital data must be "linearized", i.e., it must be made proportional to the temperature rather than to the voltage.

This language does not discuss varying a piecewise linear approximation as a function of transistor temperature. Thus, applicant submits that Bishop does not teach or suggest this step.

The third step required by this claim is the step of averaging the temperature varying, piecewise linear approximation to generate an estimate of transistor junction temperature. Col. 1, ll. 25-28 of Bishop is cited by the examiner as teaching this step. Once again, a review of the cited language indicates that it simply does not support the examiner's position in this regard. The cited portion reads:

> To achieve linearization, the frequency of these pulses is modified and made proportional to the average voltage slope over each of a plurality of segments into which the temperature-voltage curve is divided.

This language fails to even mention averaging a piecewise linear approximation in order to generate an estimate of something and certainly does not discuss averaging a temperature varying, piecewise linear approximation to generate an estimate of transistor junction temperature as required by this claim. For these reasons, applicant submits that Bishop does not teach or suggest this third step of Claim 21.

New Claims 22-23

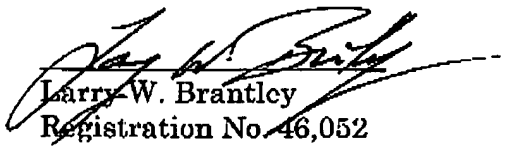
New Claims 22-23 have been added because they further distinguish the protection circuit of Claim 1 from the prior art relied upon by the examiner. Claim 22 indicates that the protection circuit of Claim 1 includes ***a transistor temperature adjustment circuit that is adapted to cause the transistor power estimation circuit to generate a power estimate that varies as a function of a temperature associated with a power transistor***. Claim 23 indicates that the protection circuit of Claim 1 includes ***a transistor temperature adjustment circuit that is adapted to cause the transistor control circuit to generate a control signal that varies as a function of a temperature associated with a power transistor***. None of the prior art relied upon by the examiner teaches or suggests the use of these types of circuits.

Applicant has commented on some of the distinctions between the cited references and the claims to facilitate a better understanding of the present invention. This discussion is not exhaustive of the facets of the invention, and Applicant hereby reserves the right to present additional distinctions as appropriate. Furthermore, while these remarks may employ shortened, more

specific, or variant descriptions of some of the claim language, Applicant respectfully notes that these remarks are not to be used to create implied limitations in the claims and only the actual wording of the claims should be considered against these references.

The Commissioner is authorized to charge any deficiency or credit any overpayment associated with the filing of this Response to Deposit Account 23-0035.

Respectfully submitted,



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CERTIFICATE OF TRANSMISSION

I hereby certify that this Response and Amendment in Application Serial No. 10/606,530 having a filing date of June 26, 2003 is being facsimile transmitted to the United States Patent and Trademark Office,. Fax No. (571) 273-8300 on December 28, 2005.

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December 28, 2005
Date